- **Operating Voltage Range of 4.5 V to 5.5 V**
- **High-Current Outputs Drive Up To 15 LSTTL Loads**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **Typical t_{pd} = 12 ns**

- **$\pm$6-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Inputs Are TTL-Voltage Compatible**
- **High-Current 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**

SN54HCT125 . . . J OR W PACKAGE
SN74HCT125 . . . D OR N PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	14	V_{CC}
1A	2	13	4$\overline{OE}$
1Y	3	12	4A
2$\overline{OE}$	4	11	4Y
2A	5	10	3$\overline{OE}$
2Y	6	9	3A
GND	7	8	3Y
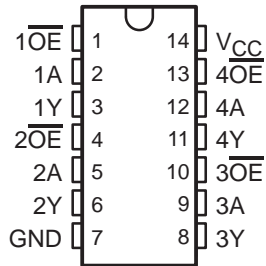
SN54HCT125 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1A, 1$\overline{OE}$, NC, V_{CC}, 4$\overline{OE}$ (pins 3, 2, 1, 20, 19)

1Y	4	18	4A
NC	5	17	NC
2$\overline{OE}$	6	16	4Y
NC	7	15	NC
2A	8	14	3$\overline{OE}$

Bottom pins: 2Y, GND, NC, 3Y, 3A (pins 9, 10, 11, 12, 13)
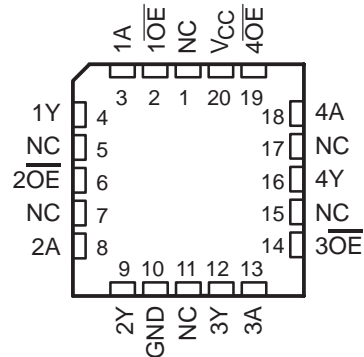
NC – No internal connection

description/ordering information

These bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube of 25	SN74HCT125N	SN74HCT125N
	SOIC – D	Tube of 50	SN74HCT125D	HCT125
		Reel of 2500	SN74HCT125DR	
		Reel of 250	SN74HCT125DT	
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCT125J	SNJ54HCT125J
	CFP – W	Tube of 150	SNJ54HCT125W	SNJ54HCT125W
	LCCC – FK	Tube of 55	SNJ54HCT125FK	SNJ54HCT125FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)
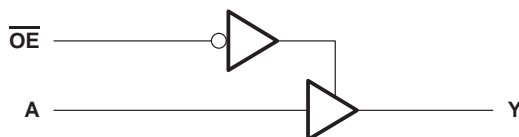
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
N package	80°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT125			SN74HCT125			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu A$	4.5 V	4.4	4.499		4.4		4.4		V
		$I_{OH} = -6\ mA$		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu A$	4.5 V		0.001	0.1		0.1		0.1	V
		$I_{OL} = 6\ mA$			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0, $V_I = V_{IH}$ or V_{IL}		5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$		5.5 V			8		160		80	μA
ΔI_{CC}†	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10*		10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		15	26		39		33	ns
			5.5 V		12	23		35		30	
t_{en}	$\overline{OE}$	Y	4.5 V		18	28		42		35	ns
			5.5 V		15	25		38		31	
t_{dis}	$\overline{OE}$	Y	4.5 V		15	26		39		33	ns
			5.5 V		13	23		35		30	
t_t		Any	4.5 V		8	15		22		19	ns
			5.5 V		7	14		21		17	

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			SN54HCT125		SN74HCT125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5 V		19	36		58		46	ns
			5.5 V		16	32		48		42	
t_{en}	$\overline{OE}$	Y	4.5 V		25	40		60		50	ns
			5.5 V		21	35		53		43	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	35	pF

TEXAS INSTRUMENTS

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PARAMETER MEASUREMENT INFORMATION
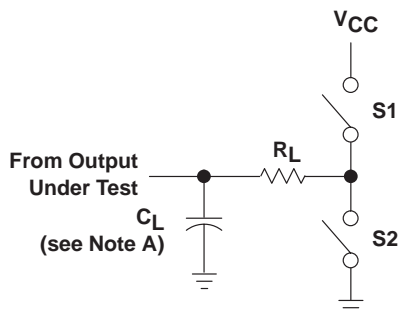
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open

LOAD CIRCUIT
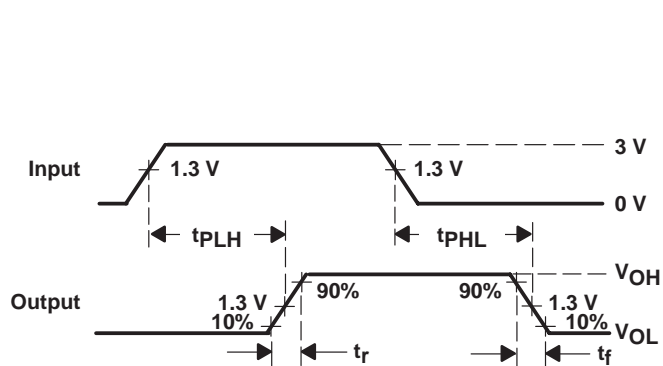
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
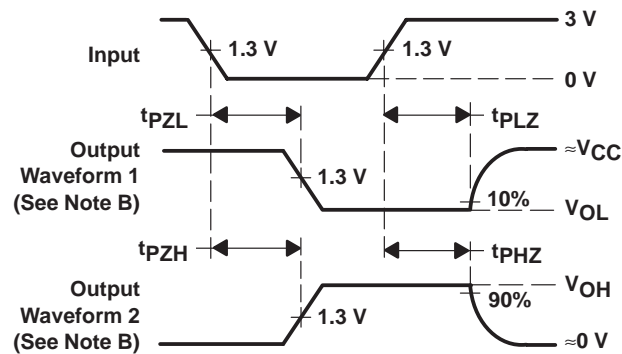
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS
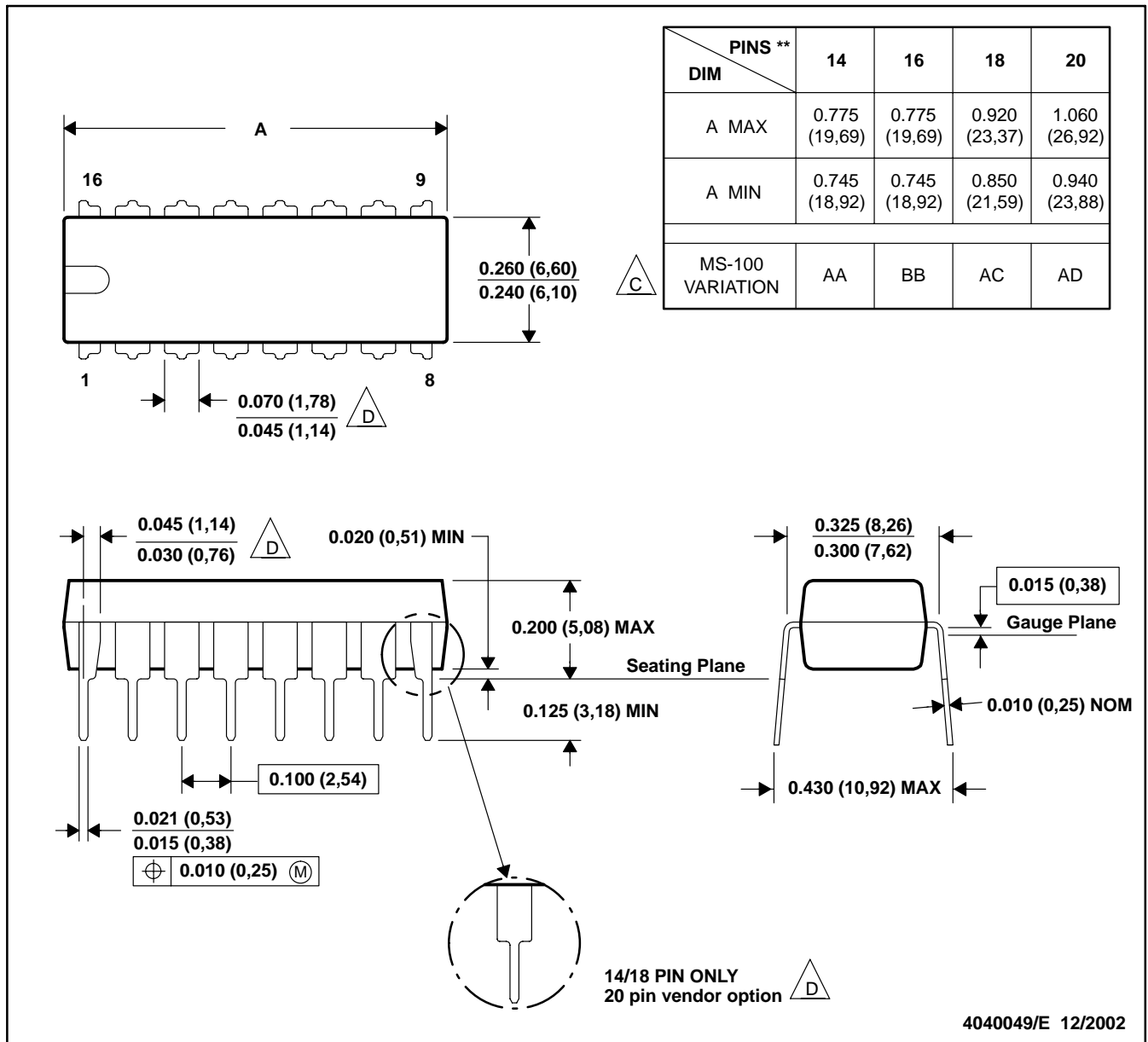
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

MECHANICAL

N (R-PDIP-T**)   **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60) / 0.240 (6,10) △C

1   8

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 PIN ONLY
20 pin vendor option △D

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
    △C Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).
    △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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D (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN

DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS-012

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